FSC-BT618

Bluetooth 5.1 Specifications Wireless MCU Module Datasheet

Version 1.0

Revision History

Version	Data	Notes	
1.0	2020/02/10	Initial Version	Devin Wan

Contact Us

Shenzhen Feasycom Technology Co.,LTD

Email: sales@feasycom.com

Address: Room 2004-2005,20th Floor,Huichao Technology Building,Jinhai Road,
Xixiang ,Baoan District,Shenzhen,518100,China.
Tel: 86-755-27924639, 86-755-23062695

Contents

1. INTRODUCTION

Overview

FSC-BT618 is a wireless MCU targeting Bluetooth 4.2 and 5.1 Low Energy applications.

FSC-BT618 is a member of the SimpleLink MCU(TI) platform of cost-effective, ultra-low power, 2.4GHz and Sub-1GHz RF devices. Very low active RF and microcontroller (MCU) currents, in addition to sub µA sleep current with up to 80KB of parity protected RAM retention, provide excellent battery lifetime and allow operation on small coin-cell batteries and in energy-harvesting applications.

FSC-BT618 combines a flexible, very low-power RF transceiver with a powerful 48MHz Arm Cortex-M4F CPU in a platform supporting multiple physical layers and RF standards. A dedicated Radio Controller (Arm Cortex-M0) handles low-level RF protocol commands that are stored in ROM or RAM, thus ensuring ultra-low power and great flexibility. The low power consumption of the FSC-BT618 does not come at the expense of RF performance; the FSC-BT618 has excellent sensitivity and robustness (selectivity and blocking) performance.

It supports GAP, ATT/GATT, SMP, L2CAP profiles. It integrates Baseband controller in a small package (Integrated chip antenna), so the designers can have better flexibilities for the product shapes.

Features

- Radio section
  - – 2.4-GHz RF transceiver compatible with Bluetooth 5.1 Low Energy
  - – Excellent receiver sensitivity (Max.):
    - –>105 dBm for Bluetooth 125-kbps (LE Coded PHY)
    - –>97 dBm for 1-Mbps PHY
  - – Output power up to +5 dBm with temperature compensation
  - – Suitable for systems targeting compliance with worldwide radio frequency regulations
    - –> EN 300 328, (Europe)
    - –>EN 300 440 Category 2
    - –> FCC CFR47 Part 15
    - – >ARIB STD-T66 (Japan)
- Supports Over-the-Air upgrade (OTA)
- Ultra-Low Power Sensor Controller with 4KB of SRAM
  - – Sample, store, and process sensor data
  - – Operation independent from system CPU
  - – Fast wake-up for low-power operation
- RoHS-compliant package
- Postage stamp sized form factor,
- Peripherals
  - – Digital peripherals can be routed to any GPIO
  - – 4× 32-bit or 8× 16-bit general-purpose timers
  - – 12-Bit ADC, 200k Samples/s, 8 channels
  - – 2× comparators with internal reference DAC (1× continuous time, 1× ultra-low power)
  - – Programmable current source
  - – UART
  - – SSI (SPI, MICROWIRE, TI)
  - – I2C
  - – I2S
  - – Real-Time Clock (RTC)
  - – AES 128- and 256-bit Crypto Accelerator
  - – ECC and RSA Public Key Hardware Accelerator

– SHA2 Accelerator (Full suite up to SHA-512)

– True Random Number Generator (TRNG)

– Capacitive sensing, up to 6 channels

– Integrated temperature and battery monitor

- External system: On-chip Buck DC/DC Converter
- Low Power

– Wide supply voltage range: 1.8 V to 3.8 V

– Active-Mode RX: 6.9 mA

– Active-Mode TX 0 dBm: 7.3 mA

– Active-Mode TX 5 dBm: 9.6 mA

– Active-Mode MCU 48 MHz (CoreMark): 3.4 mA (71 µA/MHz)

– Sensor Controller, Low Power-Mode, 2 MHz, running infinite loop: 30.8 µA

– Sensor Controller, Active-Mode, 24 MHz, running infinite loop: 808 µA

– Standby: 0.94 µA (RTC on, 80KB RAM and CPU retention)

– Shutdown: 150 nA (wakeup on external events)

- The default UART Baud rate is 115.2Kbps and can support from 1200bps up to 3Mbps
- Bluetooth stack profiles support: LE HID, and all BLE protocols.

Application

- Consumer electronics
- Mobile phone accessories
- Sports and fitness equipment
- HID applications
- Medical
- Smart grid and automatic meter reading
- Home and building automation
- Wireless alarm and security systems
- Industrial monitoring and control
- Wireless healthcare applications
- Wireless sensor networks
- Active RFID
- Energy harvesting applications
- Electronic Shelf Label (ESL)
- Long-range sensor applications

Module picture as below showing

TBD

Figure 1: FSC-BT618 Picture

2. General Specification

Table 1: General Specifications

Categories	Features	Implementation
Wireless Specification	Chip	TI CC2642R
	Bluetooth Version	Bluetooth low energy (BLE) 4.2 and 5.1 Specifications
	Frequency	2.402 - 2.480 GHz
	Transmit Power	+5 dBm (Maximum)
	Receive Sensitivity	105 dBm for Bluetooth 125-kbps (LE Coded PHY) (Maximum) 97 dBm for 1-Mbps PHY (Maximum)
	Raw Data Rates (Air)	2 Mbps(Bluetooth 5.1)
	Modulation	GFSK
	Features	LE 2-Mbit PHY (High Speed) LE Coded PHY (Long Range) Advertising Extensions Multiple Advertisement Sets CSA#2 Direction Finding / AoA
Host Interface and Peripherals	UART Interface	TX, RX, CTS, RTS
		General Purpose I/O
		Default 115200,N,8,1
		Baudrate support from 1200bps to 3Mbps
		5, 6, 7, 8 data bit character
	GPIO	22(maximum – configurable) lines
		O/P drive strength (4 mA)
		Pull-up resistor (33 KΩ) control
		Read pin-level
	I2C Interface	1 (configurable from GPIO total). Up to 400 kbps
	SSI Interface	Up to 2 SSI interfaces with a frequency of up to 4 MHz
		Support both master and slave mode
		SPI, MICROWIRE, TI
	ADC Interface	Analog input voltage range: 0V ~ 3.8V
		Supports single 12-bit SAR ADC conversion
		6 channels (configured from GPIO total)
		Up to 200MSPS conversion
	I2S Interface	handle digital audio
		pulse-density modulation microphones (PDM)
Profiles	Classic Bluetooth	No Support
	Bluetooth Low Energy	GATT Client & Peripheral - Any Custom Services
		BT5.1 Specifications
		MFI Support
Maximum Connections	Classic Bluetooth	No Support
	Bluetooth Low Energy	1Clients(TBD)

FW upgrade		Over the Air
		Xds
Supply Voltage	Supply	1.8V ~ 3.8V
Power Consumption		Active-Mode RX: 6.9 mA
		Active-Mode TX 0 dBm: 7.3 mA
		Active-Mode TX 5 dBm: 9.6 mA
		Active-Mode MCU 48 MHz (CoreMark): 3.4 mA (71 µA/MHz)
		Sensor Controller, Low Power-Mode, 2 MHz, running infinite loop: 30.8 µA
		Sensor Controller, Active-Mode, 24 MHz, running infinite loop: 808 µA
		Standby: 0.94 µA (RTC on, 80KB RAM and CPU retention)
		Shutdown: 150 nA (wakeup on external events)
Physical	Dimensions	13mm X 26.9mm X 2.0mm; Pad Pitch 1.5mm
Environmental	Operating	-40°C to +105°C
	Storage	-40°C to +150°C
Miscellaneous	Lead Free	Lead-free and RoHS compliant
	Warranty	One Year
Humidity		10% ~ 90% non-condensing
MSL grade:		MSL 3
ESD grade:	Human Body Model	All pins: ±2000V
	Charged device model	All pins: ±500V

3. HARDWARE SPECIFICATION

3.1 Block Diagram and PIN Diagram

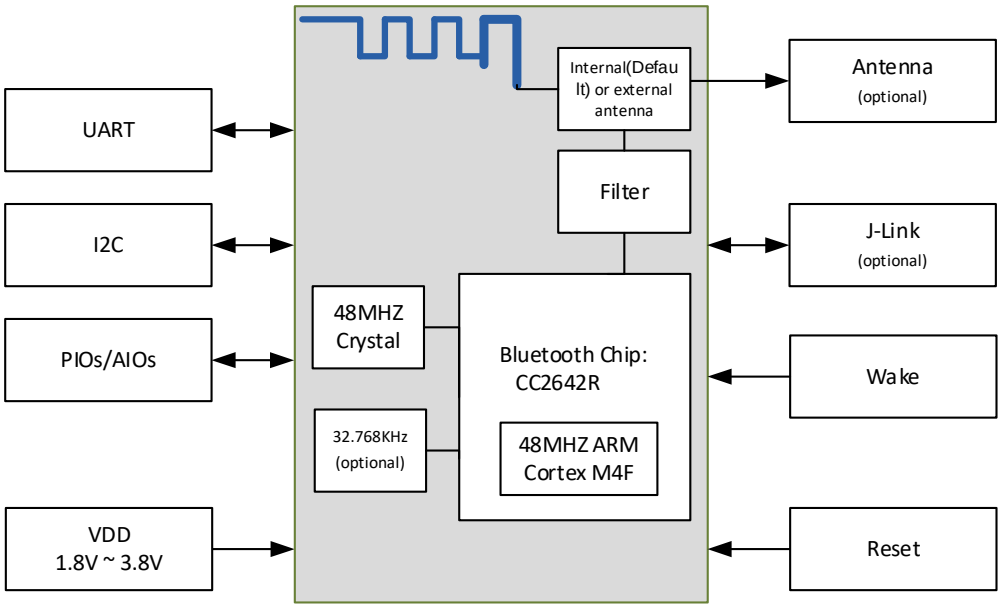


Figure 2: Block Diagram

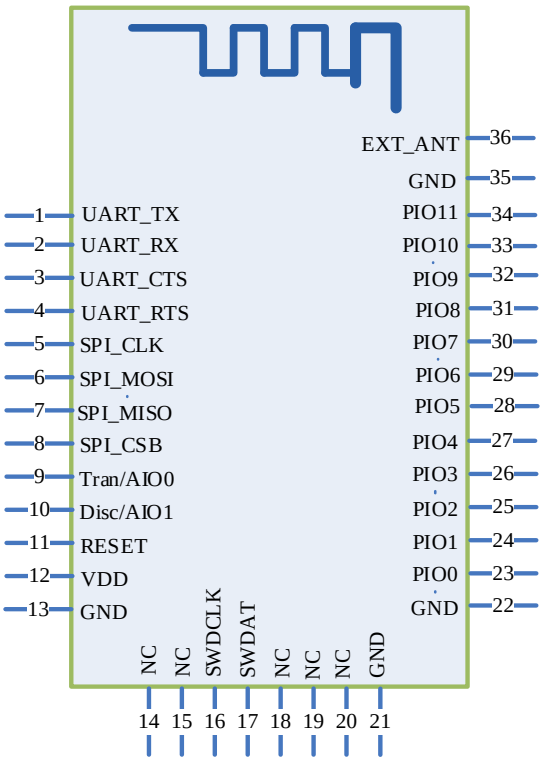


Figure 3: FSC-BT618 PIN Diagram(Top View)

3.2 PIN Definition Descriptions

Table 2: Pin definition

Pin	Pin Name	Type	Pin Descriptions	Notes
1	UART_TX	O	UART data output	Note 1
2	UART_RX	I	UART data input	Note 1
3	UART_CTS	I	UART clear to send active low	Note 1
4	UART_RTS	O	UART request to send active low	Note 1
5	SPI_CLK	I/O	Serial Peripheral Interface Clock	Note 1
6	SPI_MOSI	O	Serial Peripheral Interface Data Output	Note 1
7	SPI_MISO	I	Serial Peripheral Interface Data Input	Note 1
8	SPI_CSB	I/O	Chip Select For Synchronous Serial Interface	Note 1
9	Tran/AIO0	I/O	Programmable input/output line Alternative Function 1: Analogue programmable I/O line. Alternative Function 2: Host MCU change UART transmission mode.	Note 1
10	Disc/AIO1	I/O	Programmable input/output line Alternative Function 1: Analogue programmable I/O line. Alternative Function 2: Host MCU disconnect bluetooth.	Note 1
11	RESET	I	External reset input: Active LOW, with an inter an internal pull-up. Set this pin low reset to initial state.	
12	VDD	Vdd	Power supply voltage 1.8V ~ 3.8V	
13	GND	Vss	Power Ground	
14	NC		NC	
15	NC		NC	
16	SWDCLK	I/O	Debugging through the clk line(Default)	Note 1
17	SWDAT	I/O	Debugging through the data line(Default)	Note 1
18	NC		NC	
19	NC		NC	
20	NC		NC	
21	GND	Vss	Power Ground	
22	GND	Vss	Power Ground	
23	PIO0	I/O	Programmable input/output line	
24	PIO1	I/O	Programmable input/output line	
25	PIO2	I/O	Programmable input/output line	
26	PIO3	I/O	Programmable input/output line	
27	PIO4	I/O	Programmable input/output line	
28	PIO5	I/O	Programmable input/output line	
29	PIO6	I/O	Programmable input/output line Alternative Function: I2C CLK line (Default)	Note 1,3
30	PIO7	I/O	Programmable input/output line Alternative Function: I2C DATA line (Default)	Note 1,3
31	PIO8	I/O	Programmable input/output line	
32	PIO9	I/O	Programmable input/output line	Note

			Alternative Function: LED(Default)	1,4
33	PIO10	I/O	Programmable input/output line Alternative Function: BT Status(Default)	Note 1,2
34	PIO11	I/O	Programmable input/output line	
35	GND	Vss	RF Ground	
36	EXT_ANT	O	RF signal output	Note 5

Module Pin Notes:

Note 1	For customized module, this pin can be work as I/O Interface.
Note 2	BT Status(Default)-- Disconnected: Low Level; Connected: High Level.
Note 3	I2C Serial Clock and Data. It is essential to remember that pull-up resistors on both SCL and SDA lines are not provided in the module and MUST be provided external to the module.
Note 4	LED(Default)-- Power On: Light Slow Shinning ; Connected: Steady Lighting.
Note 5	By default, this PIN is an empty feet. This PIN can connect to an external antenna to improve the Bluetooth signal coverage. If you need to use an external antenna, by modifying the module on the 0R resistance to block out the on-board antenna; Or contact Feasycom for modification.

4. PHYSICAL INTERFACE

4.1 Power Supply

The transient response of the regulator is important. If the power rails of the module are supplied from an external voltage source, the transient response of any regulator used should be 20μs or less. It is essential that the power rail recovers quickly.

4.2 Reset

The module may be reset from several sources: Power-on Reset (POR), Low level on the nRESET Pin (nRST), Watchdog time-out reset (WDT), Low voltage reset (LVR) or Software Reset(SYSRESETREQ, CPU Reset, CHIPRST).

The RESET pin is an active low reset and is internally filtered using the internal low frequency clock oscillator. A reset will be performed between 1.5 and 4.0ms following RESET being active. It is recommended that RESET be applied for a period greater than 5ms.

At reset the digital I/O pins are set to inputs for bi-directional pins and outputs are tri-state. The PIOs have weak pull-ups.

4.3 Radio (RF Core)

The RF Core is a highly flexible and future proof radio module which contains an Arm Cortex-M0 processor that interfaces the analog RF and base-band circuitry, handles data to and from the system CPU side, and assembles the

information bits in a given packet structure. The RF core offers a high level, command-based API to the main CPU that configurations and data are passed through. The Arm Cortex- M0 processor is not programmable by customers and is interfaced through the TI-provided RF driver that is included with the SimpleLink Software Development Kit (SDK).

The RF core can autonomously handle the time-critical aspects of the radio protocols, thus offloading the main CPU, which reduces power and leaves more resources for the user application. Several signals are also available to control external circuitry such as RF switches or range extenders autonomously.

The various physical layer radio formats are partly built as a software defined radio where the radio behavior is either defined by radio ROM contents or by non-ROM radio formats delivered in form of firmware patches with the SimpleLink SDKs. This allows the radio platform to be updated for support of future versions of standards even with over-the-air (OTA) updates while still using the same silicon.

4.3.1 Bluetooth 5 low energy

The RF Core offers full support for Bluetooth 5 low energy, including the high-sped 2-Mbps physical layer and the 500-kbps and 125-kbps long range PHYs (Coded PHY) through the TI provided Bluetooth 5 stack or through a high-level Bluetooth API. The Bluetooth 5 PHY and part of the controller are in radio and system ROM, providing significant savings in memory usage and more space available for applications.

The new high-speed mode allows data transfers up to 2 Mbps, twice the speed of Bluetooth 4.2 and five times the speed of Bluetooth 4.0, without increasing power consumption. In addition to faster speeds, this mode offers significant improvements for energy efficiency and wireless coexistence with reduced radio communication time.

Bluetooth 5 also enables unparalleled flexibility for adjustment of speed and range based on application needs, which capitalizes on the high-speed or long-range modes respectively. Data transfers are now possible at 2 Mbps, enabling development of applications using voice, audio, imaging, and data logging that were not previously an option using Bluetooth low energy. With high-speed mode, existing applications deliver faster responses, richer engagement, and longer battery life. Bluetooth 5 enables fast, reliable firmware updates.

4.4 Memory

The up to 352-KB nonvolatile (Flash) memory provides storage for code and data. The flash memory is insystem programmable and erasable. The last flash memory sector must contain a Customer Configuration section (CCFG) that is used by boot ROM and TI provided drivers to configure the device. This configuration is done through the ccfg.c source file that is included in all TI provided examples.

The ultra-low leakage system static RAM (SRAM) is split into up to five 16-KB blocks and can be used for both storage of data and execution of code. Retention of SRAM contents in Standby power mode is enabled by default and included in Standby mode power consumption numbers. Parity checking for detection of bit errors in memory is built-in, which reduces chip-level soft errors and thereby increases reliability. System SRAM is always initialized to zeroes upon code execution from boot.

To improve code execution speed and lower power when executing code from nonvolatile memory, a 4-way nonassociative 8-KB cache is enabled by default to cache and prefetch instructions read by the system CPU. The cache can be used as a general-purpose RAM by enabling this feature in the Customer Configuration Area (CCFG).

There is a 4-KB ultra-low leakage SRAM available for use with the Sensor Controller Engine which is typically used for storing Sensor Controller programs, data and configuration parameters. This RAM is also accessible by the system CPU.

The Sensor Controller RAM is not cleared to zeroes between system resets.

The ROM includes a TI-RTOS kernel and low-level drivers, as well as significant parts of selected radio stacks, which frees up flash memory for the application. The ROM also contains a serial (SPI and UART) bootloader that can be used for initial programming of the device.

4.5 Sensor Controller

The Sensor Controller contains circuitry that can be selectively enabled in both Standby and Active power modes. The peripherals in this domain can be controlled by the Sensor Controller Engine, which is a proprietary power-optimized CPU. This CPU can read and monitor sensors or perform other tasks autonomously; thereby significantly reducing power consumption and offloading the system CPU.

The Sensor Controller Engine is user programmable with a simple programming language that has syntax similar to C. This programmability allows for sensor polling and other tasks to be specified as sequential algorithms rather than static configuration of complex peripheral modules, timers, DMA, register programmable state machines, or event routing.

The main advantages are:

- Flexibility - data can be read and processed in unlimited manners while still ensuring ultra-low power
- 2 MHz low-power mode enables lowest possible handling of digital sensors
- Dynamic reuse of hardware resources
- 40-bit accumulator supporting multiplication, addition and shift
- Observability and debugging options

Sensor Controller Studio is used to write, test, and debug code for the Sensor Controller. The tool produces C driver source code, which the System CPU application uses to control and exchange data with the Sensor Controller. Typical use cases may be (but are not limited to) the following:

- Read analog sensors using integrated ADC or comparators
- Interface digital sensors using GPIOs, SPI, UART, or I2C (UART and I2C are bit-banged)
- Capacitive sensing
- Waveform generation
- Very low-power pulse counting (flow metering)
- Key scan

The peripherals in the Sensor Controller include the following:

- The low-power clocked comparator can be used to wake the system CPU from any state in which the comparator is active. A configurable internal reference DAC can be used in conjunction with the comparator. The output of the comparator can also be used to trigger an interrupt or the ADC.
- Capacitive sensing functionality is implemented through the use of a constant current source, a time to-digital converter, and a comparator. The continuous time comparator in this block can also be used as a higher-accuracy

alternative to the low-power clocked comparator. The Sensor Controller takes care of baseline tracking, hysteresis, filtering, and other related functions when these modules are used for capacitive sensing.

- The ADC is a 12-bit, 200-ksamples/s ADC with eight inputs and a built-in voltage reference. The ADC can be triggered by many different sources including timers, I/O pins, software, and comparators.
- The analog modules can connect to up to eight different GPIOs
- Dedicated SPI master with up to 6 MHz clock speed

The peripherals in the Sensor Controller can also be controlled from the main application processor.

4.6 Cryptography

FSC-BT618 comes with a wide set of modern cryptography-related hardware accelerators, drastically reducing code footprint and execution time for cryptographic operations. It also has the benefit of being lower power and improves availability and responsiveness of the system because the cryptography operations runs in a background hardware thread.

Together with a large selection of open-source cryptography libraries provided with the Software Development Kit (SDK), this allows for secure and future proof IoT applications to be easily built on top of the platform. The hardware accelerator modules are:

- **True Random Number Generator (TRNG)** module provides a true, nondeterministic noise source for the purpose of generating keys, initialization vectors (IVs), and other random number requirements. The TRNG is built on 24 ring oscillators that create unpredictable output to feed a complex nonlinear combinatorial circuit.
- **Secure Hash Algorithm 2 (SHA-2)** with support for SHA224, SHA256, SHA384, and SHA512
- **Advanced Encryption Standard (AES)** with 128 and 256 bit key lengths
- **Public Key Accelerator** - Hardware accelerator supporting mathematical operations needed for elliptic curves up to 512 bits and RSA key pair generation up to 1024 bits.

Through use of these modules and the TI provided cryptography drivers, the following capabilities are available for an application or stack:

- **Key Agreement Schemes**
  – Elliptic curve Diffie–Hellman with static or ephemeral keys (ECDH and ECDHE)
  – Elliptic curve Password Authenticated Key Exchange by Juggling (ECJ-PAKE)
- **Signature Generation**
  – Elliptic curve Diffie-Hellman Digital Signature Algorithm (ECDSA)
- **Curve Support**
  – Short Weierstrass form (full hardware support), such as:
    - NIST-P224, NIST-P256, NIST-P384, NIST-P521

- Brainpool-256R1, Brainpool-384R1, Brainpool-512R1
- secp256r1

– Montgomery form (hardware support for multiplication), such as:

- Curve25519

- **SHA2 based MACs**

– HMAC with SHA224, SHA256, SHA384, or SHA512

- Block cipher mode of operation

– AESCCM

– AESGCM

– AESECB

– AESCBC

– AESCBC-MAC

- **True random number generation**

Other capabilities, such as RSA encryption and signatures as well as Edwards type of elliptic curves such as Curve1174 or Ed25519, can also be implemented using the provided hardware accelerators but are not part of the TI SimpleLink SDK for the CC2642R device.

4.7 Timers

A large selection of timers are available as part of the CC2642R device. These timers are:

- **Real-Time Clock (RTC)**

A 70-bit 3-channel timer running on the 32 kHz low frequency system clock (SCLK_LF). This timer is available in all power modes except Shutdown. The timer can be calibrated to compensate for frequency drift when using the LF RCOSC as the low frequency system clock. If an external LF clock with frequency different from 32.768 kHz is used, the RTC tick speed can be adjusted to compensate for this. When using TI-RTOS, the RTC is used as the base timer in the operating system and should thus only be accessed through the kernel APIs such as the Clock module. The real time clock can also be read by the Sensor Controller Engine to timestamp sensor data and also has dedicated capture channels. By default, the RTC halts when a debugger halts the device.

- **General Purpose Timers (GPTIMER)**

The four flexible GPTIMERs can be used as either 4× 32 bit timers or 8× 16 bit timers, all running on up to 48 MHz. Each of the 16- or 32-bit timers support a wide range of features such as one-shot or periodic counting, pulse width modulation (PWM), time counting between edges and edge counting.

The inputs and outputs of the timer are connected to the device event fabric, which allows the timers to interact with signals such as GPIO inputs, other timers, DMA and ADC. The GPTIMERs are available in Active and Idle power modes.

- **Sensor Controller Timers**

The Sensor Controller contains 3 timers:

AUX Timer 0 and 1 are 16-bit timers with a 2N prescaler. Timers can either increment on a clock or on each edge of a

selected tick source. Both one-shot and periodical timer modes are available.

AUX Timer 2 is a 16-bit timer that can operate at 24 MHz, 2 MHz or 32 kHz independent of the Sensor Controller functionality. There are 4 capture or compare channels, which can be operated in one-shot or periodical modes. The timer can be used to generate events for the Sensor Controller Engine or the ADC, as well as for PWM output or waveform generation.

- **Radio Timer**

A multichannel 32-bit timer running at 4 MHz is available as part of the device radio. The radio timer is typically used as the timing base in wireless network communication using the 32-bit timing word as the network time. The radio timer is synchronized with the RTC by using a dedicated radio API when the device radio is turned on or off. This ensures that for a network stack, the radio timer seems to always be running when the radio is enabled. The radio timer is in most cases used indirectly through the trigger time fields in the radio APIs and should only be used when running the accurate 48 MHz high frequency crystal is the source of SCLK_HF.

- **Watchdog timer**

The watchdog timer is used to regain control if the system operates incorrectly due to software errors. It is typically used to generate an interrupt to and reset of the device for the case where periodic monitoring of the system components and tasks fails to verify proper functionality. The watchdog timer runs on a 1.5 MHz clock rate and cannot be stopped once enabled. The watchdog timer pauses to run in Standby power mode and when a debugger halts the device.

4.8 Serial Peripherals and I/O

The SSIs are synchronous serial interfaces that are compatible with SPI, MICROWIRE, and TI's synchronous serial interfaces. The SSIs support both SPI master and slave up to 4MHz. The SSI modules support configurable phase and polarity.

The UARTs implement universal asynchronous receiver and transmitter functions. They support flexible baud-rate generation up to a maximum of 3 Mbps.

The I^2S interface is used to handle digital audio and can also be used to interface pulse-density modulation microphones (PDM).

The I^2C interface is also used to communicate with devices compatible with the I^2C standard. The I^2C interface can handle 100 kHz and 400 kHz operation, and can serve as both master and slave.

The I/O controller (IOC) controls the digital I/O pins and contains multiplexer circuitry to allow a set of peripherals to be assigned to I/O pins in a flexible manner. All digital I/Os are interrupt and wake-up capable, have a programmable pullup and pulldown function, and can generate an interrupt on a negative or positive edge (configurable). When configured as an output, pins can function as either push-pull or open-drain. Five GPIOs have high-drive capabilities, which are marked in bold in **Figure 3**. All digital peripherals can be connected to any digital pin on the device.

4.8.1 UART

FSC-BT618 provides one channels of Universal Asynchronous Receiver/Transmitters(UART)(Full-duplex asynchronous communications). The UART Controller performs a serial-to-parallel conversion on data received from the peripheral and a parallel-to-serial conversion on data transmitted from the CPU. Each UART Controller channel supports ten types of interrupts.

This is a standard UART interface for communicating with other serial devices. The UART interface provides a simple mechanism for communicating with other serial devices using the RS232 protocol.

When the module is connected to another digital device, UART_RX and UART_TX transfer data between the two devices. The remaining two signals, UART_CTS and UART_RTS, can be used to implement RS232 hardware flow control where both are active low indicators.

This module output is at 3.3V CMOS logic levels (tracks VCC). Level conversion must be added to interface with an RS-232 level compliant interface.

Some serial implementations link CTS and RTS to remove the need for handshaking. We do not recommend linking CTS and RTS except for testing and prototyping. If these pins are linked and the host sends data when the FSC-BT618 deasserts its RTS signal, there is significant risk that internal receive buffers will overflow, which could lead to an internal processor crash. This drops the connection and may require a power cycle to reset the module. We recommend that you adhere to the correct CTS/RTS handshaking protocol for proper operation.

Table 3: Possible UART Settings

Parameter	Possible Values	
Baudrate	Minimum	1200 baud (≤2%Error)
	Standard	115200bps(≤1%Error)
	Maximum	3Mbps(≤1%Error)
Flow control		RTS/CTS, or None
Parity		None, Odd or Even
Number of stop bits		1 /1.5/2
Bits per channel		5/6/7/8

When connecting the module to a host, please make sure to follow .

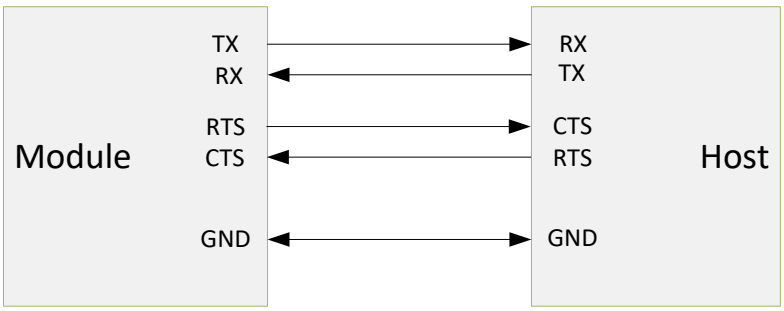


Figure 4: UART Connection

4.8.2 I²C Interface

- Up to two I²C bus interfaces can support both master and slave mode with a frequency up to 400KHZ.
- Provide arbitration function, optional PEC(packet error checking) generation and checking.
- Supports 7 –bit and 10 –bit addressing mode and general call addressing mode.

The I²C interface is an internal circuit allowing communication with an external I²C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line (SDA) and a serial clock line (SCL). The I²C module provides two data transfer rates: 100 kHz of standard mode or 400kHz of the fast mode. The I²C module also has an arbitration detect function to prevent the situation where more than one master attempts to transmit data to the I²C bus at the same time. A CRC-8 calculator is also provided in I²C interface to perform packet error checking for I²C data.

4.9 Battery and Temperature Monitor

A combined temperature and battery voltage monitor is available in the CC2642R device. The battery and temperature monitor allows an application to continuously monitor on-chip temperature and supply voltage and respond to changes in environmental conditions as needed. The module contains window comparators to interrupt the system CPU when temperature or supply voltage go outside defined windows. These events can also be used to wake up the device from Standby mode through the Always- On (AON) event fabric.

4.10 µDMA

The module includes a direct memory access (µDMA) controller. The µDMA controller provides a way to offload data-transfer tasks from the system CPU, thus allowing for more efficient use of the processor and the available bus bandwidth. The µDMA controller can perform a transfer between memory and peripherals. The µDMA controller has dedicated channels for each supported on-chip module and can be programmed to automatically perform transfers between peripherals and memory when the peripheral is ready to transfer more data.

Some features of the µDMA controller include the following (this is not an exhaustive list):

- Highly flexible and configurable channel operation of up to 32 channels
- Transfer modes: memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral
- Data sizes of 8, 16, and 32 bits
- Ping-pong mode for continuous streaming of data

5. ELECTRICAL CHARACTERISTICS

5.1 Absolute Maximum Ratings

Absolute maximum ratings for supply voltage and voltages on digital and analogue pins of the module are listed below. Exceeding these values causes permanent damage.

The average PIO pin output current is defined as the average current value flowing through any one of the corresponding pins for a 100mS period. The total average PIO pin output current is defined as the average current value flowing through all of the corresponding pins for a 100mS period. The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

Table 4: Absolute Maximum Rating

Parameter	Min	Max	Unit
V_{DD}-V_{SS} - DC Power Supply	-0.3	+4.1	V
V_{IN} - Voltage on any digital pin	-0.3	Vdd+0.3(max 4.1)	V
V_{IN} - Voltage on ADC input (Voltage scaling enabled)	-0.3	Vdd	V
V_{IN} - Voltage on ADC input (Voltage scaling disabled, VDDS as reference)	-0.3	VDD / 2.9	V
Input RF level		5	dBm
T_{ST} - Storage Temperature	-40	+150	°C
I_{IO} - Maximum Current sunk by a I/O pin		8	mA
I_{IO} - Maximum Current sourced by a I/O pin		8	mA

5.2 Recommended Operating Conditions

Table 5: Recommended Operating Conditions

Parameter	Min	Type	Max	Unit
V_{DD}-V_{SS} - DC Power Supply	1.8	3.3	3.8	V
T_A - Operating Temperature	-40	25	+105	°C
I_{IO} - Maximum Current sunk by a I/O pin	2	4	6	mA
I_{IO} - Maximum Current sourced by a I/O pin	2	4	6	mA

5.3 GPIO

Table 6: GPIO DC Characteristics

Parameter	Min	Type	Max	Unit
V_{DD} = 1.8V, T_A = 25°C				
V_{OH} - High Level Output Voltage, I_{IO}=8mA IOCURR = 2, high-drive GPIOs only	-	1.56	-	V
V_{OL} - Low Level Output Voltage, I_{IO}=8mA IOCURR = 2, high-drive GPIOs only	-	0.24	-	V

V_{OH} - High Level Output Voltage, I_{IO}=4mA , IOCURR = 1	-	1.59	-	V
V_{OL} - Low Level Output Voltage, I_{IO}=4mA , IOCURR = 1	-	0.21	-	V
GPIO pullup current - Input mode, pullup enabled, Vpad = 0 V	-	73	-	uA
GPIO pulldown current - Input mode, pulldown enabled, Vpad = VDD	-	19	-	uA
GPIO high/low input transition, no hysteresis - IH = 0, transition between reading 0 and reading 1	-	0.88	-	V
GPIO low-to-high input transition, with hysteresis - IH = 1, transition voltage for input read as 0 → 1	-	1.08	-	V
GPIO high-to-low input transition, with hysteresis - IH = 1, transition voltage for input read as 1 → 0	-	0.73	-	V
GPIO input hysteresis - IH = 1, difference between 0 → 1 and 1 → 0 points	-	0.35	-	V
V_{DD} = 3.0V, T_A = 25°C				
VOH - High Level Output Voltage, IIO=8mA IOCURR = 2, high-drive GPIOs only	-	2.59	-	V
VOL - Low Level Output Voltage, IIO=8mA IOCURR = 2, high-drive GPIOs only	-	0.42	-	V
VOH - High Level Output Voltage, IIO=4mA , IOCURR = 1	-	2.63	-	V
VOL - Low Level Output Voltage, IIO=4mA , IOCURR = 1	-	0.40	-	V
V_{DD} = 3.8V, T_A = 25°C				
GPIO pullup current - Input mode, pullup enabled, Vpad = 0 V	-	282	-	uA
GPIO pulldown current - Input mode, pulldown enabled, Vpad = VDD	-	110	-	uA
GPIO high/low input transition, no hysteresis - IH = 0, transition between reading 0 and reading 1	-	1.67	-	V
GPIO low-to-high input transition, with hysteresis - IH = 1, transition voltage for input read as 0 → 1	-	1.97	-	V
GPIO high-to-low input transition, with hysteresis - IH = 1, transition voltage for input read as 1 → 0	-	1.55	-	V
GPIO input hysteresis - IH = 1, difference between 0 → 1 and 1 → 0 points	-	0.42	-	V
T_A = 25°C				
VIH - Lowest GPIO input voltage reliably interpreted as a High	0.8	-	-	VDD
VIL - Lowest GPIO input voltage reliably interpreted as a LOW	-	-	0.2	VDD

5.4 Peripheral Characteristics

5.4.1 ADC

Table 7: Specifications of 12-bit SARADC(voltage scaling enabled, unless otherwise noted.(1))

Parameter	Min	Type	Max	Unit
V_{DDA} - Operation Voltage	0	-	3.8	V
R_{ADC} - Resolution	-	12	-	bit
F_{SPS} - Sampling Rate	-	-	200	kSamples/s
Offset (Internal 4.3-V equivalent reference(2))	-	-0.24	-	LSB
Gain error (Internal 4.3-V equivalent reference(2))	-	7.14	-	LSB
DNL(3) Differential nonlinearity	-	>–1	-	LSB
INL(4) Integral nonlinearity	-	±4	-	LSB
ENOB - Effective number of bits				
Internal 4.3-V equivalent reference(2), 200ksps,9.6-kHz input tone	-	9.8	-	bits
VDD as reference, 200 ksps, 9.6-kHz input tone	-	10.1	-	bits
Internal 1.44-V reference, voltage scaling disabled,32 samples average, 200ksps, 300-Hz input tone	-	11.1	-	bits
THD - Total harmonic distortion				
Internal 4.3-V equivalent reference(2), 200 ksps,9.6-kHz input tone	-	-65	-	dB
VDD as reference, 200ksps, 9.6-kHz input tone	-	-70	-	dB
Internal 1.44-V reference, voltage scaling disabled,32 samples average, 200ksps, 300-Hz input tone	-	-72	-	dB
SINAD,SNDR - Signal-to-noise and distortion ratio				
Internal 4.3-V equivalent reference(2), 200ksps,9.6-kHz input tone	-	60	-	dB
VDD as reference, 200ksps, 9.6-kHz input tone	-	63	-	dB
Internal 1.44-V reference, voltage scaling disabled,32 samples average, 200ksps, 300-Hz input tone	-	68	-	dB
SFDR - Spurious-free dynamic range				
Internal 4.3-V equivalent reference(2), 200ksps,9.6-kHz input tone	-	70	-	dB
VDD as reference, 200ksps, 9.6-kHz input tone	-	73	-	dB
Internal 1.44-V reference, voltage scaling disabled,32 samples average, 200ksps, 300-Hz input tone	-	75	-	dB
Conversion time - Serial conversion, time-to-output, 24-MHz clock	-	50	-	Clock-cycles
Current consumption - Internal 4.3-V equivalent reference(2)	-	0.42	-	mA
Current consumption - VDD as reference	-	0.6	-	mA
Reference voltage - Equivalent fixed internal reference (input voltage scaling enabled). For best accuracy, the ADC conversion should be initiated through the TI-RTOS API in order to include the gain/offset compensation factors stored in FCFG1	-	4.3(2) (4)	-	V
Reference voltage - Fixed internal reference (input voltage scaling disabled). For best accuracy, the ADC conversion should be initiated through the TI-RTOS		1.48		

API in order to include the gain/offset compensation factors stored in FCFG1. This value is derived from the scaled value (4.3 V) as follows: Vref = 4.3 V × 1408 / 4095					
Reference voltage - VDDS as reference, input voltage scaling enabled			VDD		
Reference voltage - VDDS as reference, input voltage scaling disabled			VDD/2.82(4)		
Input impedance - 200 ksps, voltage scaling enabled. Capacitive input, Input impedance depends on sampling frequency and sampling time		-	>1	-	MΩ

(1) Using IEEE Std 1241-2010 for terminology and test methods
(2) Input signal scaled down internally before conversion, as if voltage range was 0 to 4.3 V
(3) No missing codes
(4) Applied voltage must be within Absolute Maximum Ratings at all times

5.4.1 DAC

Table 8: Digital-to-Analog Converter (DAC) Characteristics (T_C = 25 °C, V_{DDS} = 3.0 V unless otherwise noted.)

Parameter		Test Conditions	Min	Typ	Max	Unit
General Parameters						
	Resolution			8		Bits
VDD	Supply voltage	Any load, any V_{REF}, pre-charge OFF, DAC charge-pump ON	1.8		3.8	V
		External Load(1), any V_{REF}, pre-charge OFF, DAC charge pump OFF	2.0		3.8	
		Any load, V_{REF} = DCOUPL, pre-charge ON	2.6		3.8	
F_{DAC}	Clock frequency	Buffer ON (recommended for external load)	16		250	KHz
		Buffer OFF (internal load)	16		1000	
	Voltage output settling time	V_{REF} = VDDS, buffer OFF, internal load		13		1 / F_{DAC}
		V_{REF} = VDDS, buffer ON, external capacitive load = 20 pF(2)		13.8		
	External capacitive load			20	200	pF
	External resistive load		10			MΩ
	Short circuit current				400	uA
Z_{MAX}	Max output impedance Vref = VDDS, buffer ON, CLK 250 kHz	VDDS = 3.8 V, DAC charge-pump OFF		50.8		kΩ
		VDDS = 3.0 V, DAC charge-pump ON		51.7		
		VDDS = 3.0 V, DAC charge-pump OFF		53.2		
		VDDS = 2.0 V, DAC charge-pump ON		48.7		

		VDDS = 2.0 V, DAC charge-pump OFF	70.2	
		VDDS = 1.8 V, DAC charge-pump ON	46.3	
		VDDS = 1.8 V, DAC charge-pump OFF	88.9	
Internal Load - Continuous Time Comparator / Low Power Clocked Comparator				
DNL	Differential nonlinearity	V_{REF} = VDDS, load = Continuous Time Comparator or Low Power Clocked Comparator FDAC = 250 kHz	±1	LSB(3)
	Differential nonlinearity	V_{REF} = VDDS, load = Continuous Time Comparator or Low Power Clocked Comparator FDAC = 16 kHz	±1.2	
	Offset error(4) Load = Continuous Time Comparator	V_{REF} F = VDDS = 3.8 V	±0.64	LSB(3)
		V_{REF} = VDDS = 3.0 V	±0.81	
		V_{REF} = VDDS = 1.8 V	±1.27	
		V_{REF} = DCOUPL, pre-charge ON	±3.43	
		V_{REF} = DCOUPL, pre-charge OFF	±2.88	
		V_{REF} = ADCREF	±2.37	
	Offset error(4) Load = Low Power Clocked Comparator	V_{REF} = VDDS = 3.8 V	±0.78	LSB(3)
		V_{REF} = VDDS = 3.0 V	±0.77	
		V_{REF} = VDDS = 1.8 V	±3.46	
		V_{REF} = DCOUPL, pre-charge ON	±3.44	
		V_{REF} = DCOUPL, pre-charge OFF	±4.70	
		V_{REF} = ADCREF	±4.11	
	Max code output voltage variation(4) Load = Continuous Time Comparator	V_{REF} = VDDS = 3.8 V	±1.53	LSB(3)
		V_{REF} = VDDS = 3.0 V	±1.71	
		V_{REF} = VDDS = 1.8 V	±2.10	
		V_{REF} = DCOUPL, pre-charge ON	±6.00	
		V_{REF} = DCOUPL, pre-charge OFF	±3.85	
		V_{REF} = ADCREF	±5.84	
	Max code output voltage variation(4) Load = Low Power Clocked Comparator	V_{REF} = VDDS = 3.8 V	±2.92	LSB(3)
		V_{REF} = VDDS = 3.0 V	±3.06	
		V_{REF} = VDDS = 1.8 V	±3.91	
		V_{REF} = DCOUPL, pre-charge ON	±7.84	
		V_{REF} = DCOUPL, pre-charge OFF	±4.06	
		V_{REF} = ADCREF	±6.94	
	Output voltage range(4) Load = Continuous Time Comparator	V_{REF} = VDDS = 3.8 V, code 1	0.03	LSB(3)
		V_{REF} = VDDS = 3.8 V, code 255	3.62	
		V_{REF} = VDDS = 3.0 V, code1	0.02	
		V_{REF} = VDDS = 3.0 V, code255	2.86	
		V_{REF} = VDDS = 1.8 V, Code 1	0.01	
		V_{REF} = VDDS = 1.8 V, Code 255	1.71	

		V_{REF} = DCOUPL, pre-charge OFF, Code 1	0.01	
		V_{REF} = DCOUPL, pre-charge OFF, Code 255	1.21	
		V_{REF} = DCOUPL, pre-charge ON, Code 1	1.27	
		V_{REF} = DCOUPL, pre-charge ON, Code 255	2.46	
		V_{REF} = ADCREF, Code 1	0.01	
		V_{REF} = ADCREF, Code 255	1.41	
	Output voltage range(4) Load = Low Power Clocked Comparator	V_{REF} = VDDS = 3.8 V, code 1	0.03	LSB(3)
		V_{REF} = VDDS = 3.8 V, code 255	3.61	
		V_{REF} = VDDS = 3.0 V, code1	0.02	
		V_{REF} = VDDS = 3.0 V, code255	2.85	
		V_{REF} = VDDS = 1.8 V, Code 1	0.01	
		V_{REF} = VDDS = 1.8 V, Code 255	1.71	
		V_{REF} = DCOUPL, pre-charge OFF, Code 1	0.01	
		V_{REF} = DCOUPL, pre-charge OFF, Code 255	1.21	
		V_{REF} = DCOUPL, pre-charge ON, Code 1	1.27	
		V_{REF} = DCOUPL, pre-charge ON, Code 255	2.46	
		V_{REF} = ADCREF, Code 1	0.01	
		V_{REF} = ADCREF, Code 255	1.41	
External Load (Keysight 34401A Multimeter)				
INL	Integral nonlinearity	V_{REF} = VDDS, FDAC = 250 kHz	±1	LSB(3)
		V_{REF} = DCOUPL, FDAC = 250 kHz	±1	
		V_{REF} = ADCREF, FDAC = 250 kHz	±1	
DNL	Differential nonlinearity	V_{REF} = VDDS, FDAC = 250 kHz	±1	LSB(3)
	Offset error	V_{REF} = VDDS = 3.8 V	±0.20	LSB(3)
		V_{REF} = VDDS = 3.0 V	±0.25	
		V_{REF} = VDDS = 1.8 V	±0.45	
		V_{REF} = DCOUPL, pre-charge ON ±1.55	±1.55	
		V_{REF} = DCOUPL, pre-charge OFF	±1.30	
		V_{REF} = ADCREF	±1.10	
	Max code output voltage variation	V_{REF} = VDDS = 3.8 V	±0.60	LSB(3)
		V_{REF} = VDDS = 3.0 V	±0.55	
		V_{REF} = VDDS = 1.8 V	±0.60	
		V_{REF} = DCOUPL, pre-charge ON ±1.55	±3.45	
		V_{REF} = DCOUPL, pre-charge OFF	±2.10	
		V_{REF} = ADCREF	±1.90	
	Output voltage range Load = Low Power Clocked Comparator	V_{REF} = VDDS = 3.8 V, code 1	0.03	LSB(3)
		V_{REF} = VDDS = 3.8 V, code 255	3.61	
		V_{REF} = VDDS = 3.0 V, code1	0.02	
		V_{REF} = VDDS = 3.0 V, code255	2.85	
		V_{REF} = VDDS = 1.8 V, Code 1	0.02	
		V_{REF} = VDDS = 1.8 V, Code 255	1.71	
		V_{REF} = DCOUPL, pre-charge OFF, Code 1	0.02	

	V_{REF} = DCOUPL, pre-charge OFF, Code 255	1.20
	V_{REF} = DCOUPL, pre-charge ON, Code 1	1.27
	V_{REF} = DCOUPL, pre-charge ON, Code 255	2.46
	V_{REF} = ADCREF, Code 1	0.02
	V_{REF} = ADCREF, Code 255	1.42

(1) Keysight 34401A Multimeter

(2) A load > 20 pF will increases the settling time

(3) 1 LSB (V_{REF} 3.8 V/3.0 V/1.8 V/DCOUPL/ADCREF) = 14.10 mV/11.13 mV/6.68 mV/4.67 mV/5.48 mV

(4) Includes comparator offset

5.5 Temperature Sensor

Table 9: Temperature Sensor (reference design with Tc = 25°C, VDD = 3.0 V, unless otherwise noted)

Parameter	Min	Type	Max	Unit
Resolution	-	2	-	°C
Accuracy - -40 °C to 0 °C		±4.0		°C
Accuracy - 0 °C to 85 °C	-	±2.5	-	°C
Supply voltage coefficient(1)	-	3.6	-	°C /V

(1) The temperature sensor is automatically compensated for VDDS variation when using the TI-provided driver.

5.6 Battery Monitor

Table 10: Battery Monitor (reference design with Tc = 25°C, VDD = 3.0 V, unless otherwise noted)

Parameter	Min	Type	Max	Unit
Resolution	-	25	-	mV
Range	1.8	-	3.8	V
Integral nonlinearity (max)	-	23	-	mV
Accuracy - DDS = 3.0 V	-	22.5	-	mV
Offset error		-32		mV
Gain error		-1		%

5.7 Synchronous Serial Interface (SSI) Characteristics

Table 11: Synchronous Serial Interface (SSI) Characteristics
over operating free-air temperature range (unless otherwise noted)

Parameter	Min	Type	Max	Unit
S1 t_{clk_per} (SSIClk cycle time)	12	-	65024	System clocks(1)
S2 t_{clk_high} (SSIClk high time)	-	0.5	-	t_{clk_per}
S3 t_{clk_low} (SSIClk low time)	-	0.5	-	t_{clk_per}

(1) When using the TI-provided Power driver, the SSI system clock is always 48 MHz.
(2) Refer to SSI timing diagrams

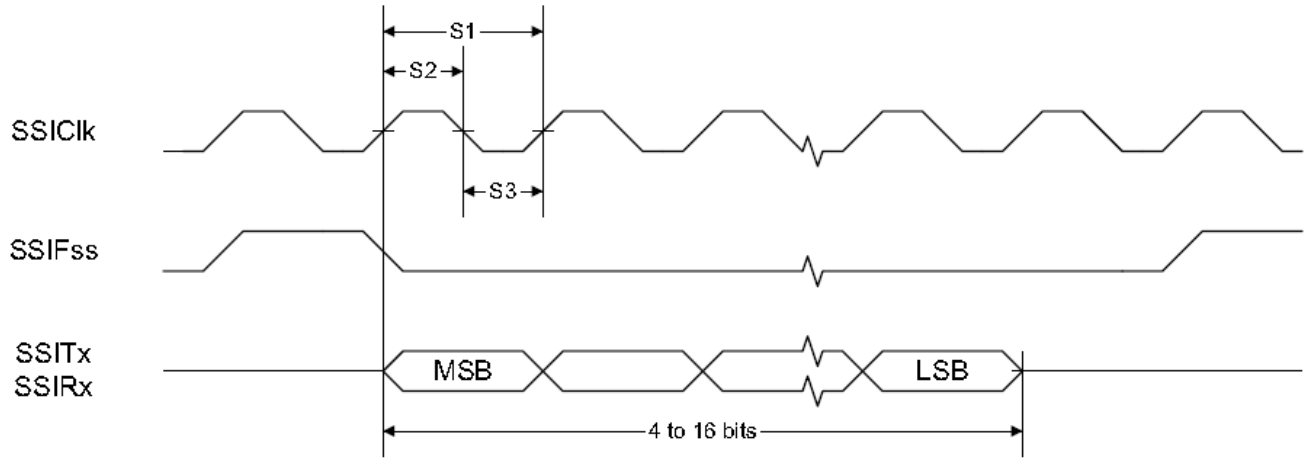


Figure 5: SSI Timing for TI Frame Format (FRF = 01), Single Transfer Timing Measurement

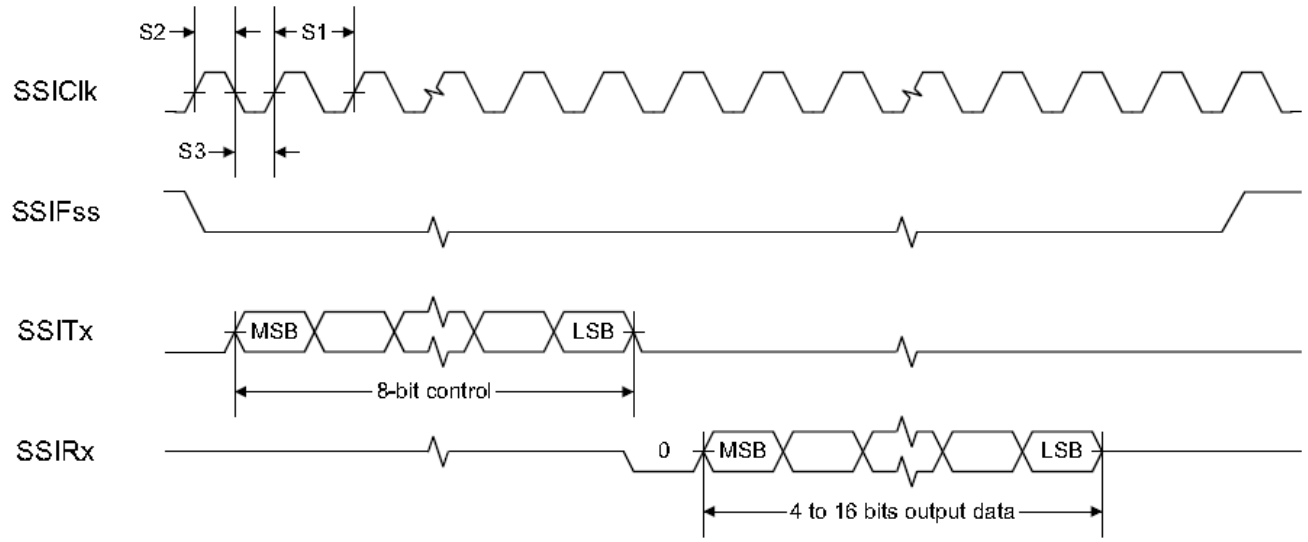


Figure 6: SSI Timing for MICROWIRE Frame Format (FRF = 10), Single Transfer

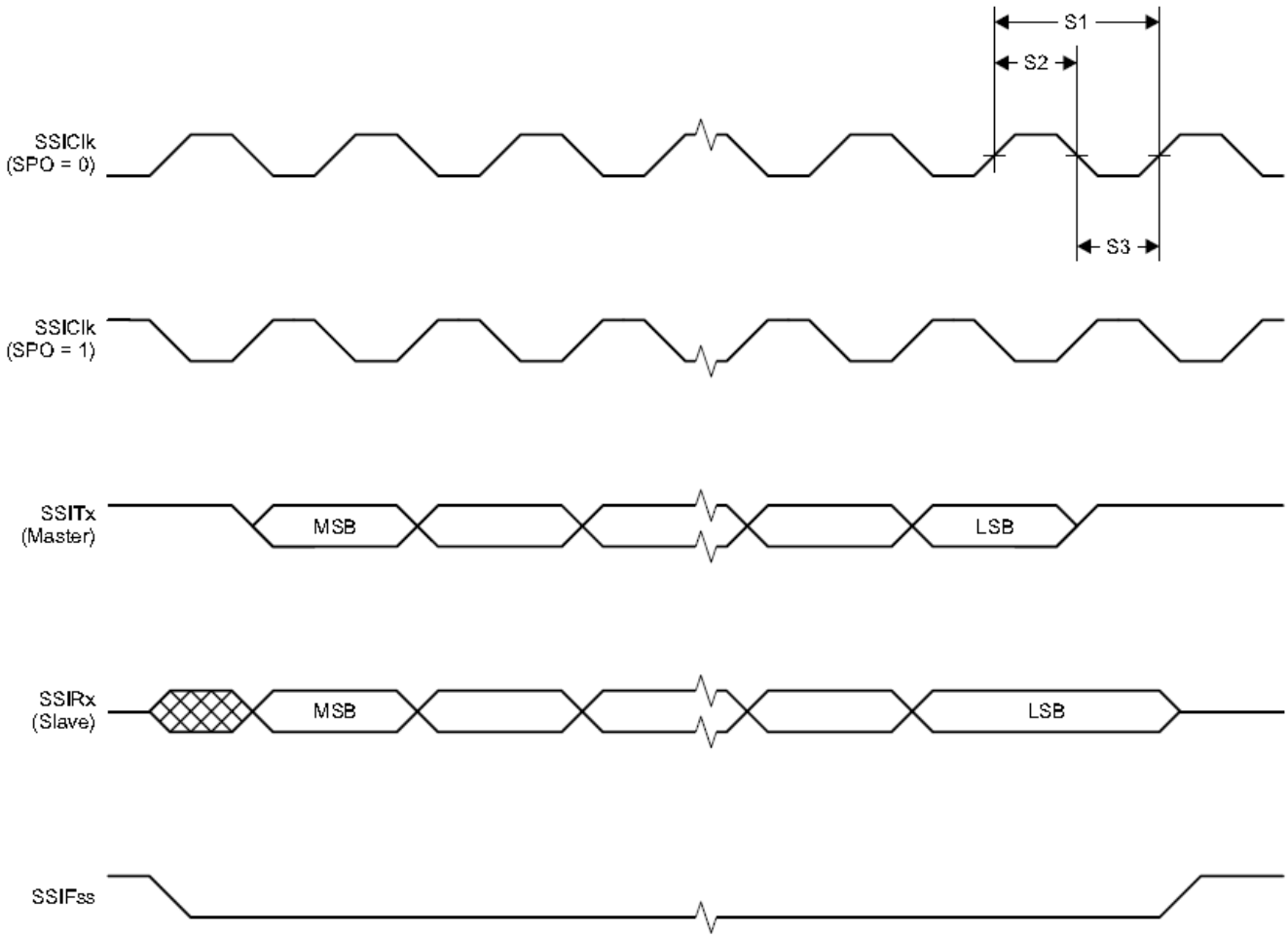


Figure 7: SSI Timing for SPI Frame Format (FRF = 00), With SPH = 1

5.8 Timing and Switching Characteristics

Table 12: Reset Timing

Parameter	Min	Typ	Max	Unit
RESET_N low duration	1			us

Table 13: Wakeup Timing

Measured over operating free-air temperature with VDDS = 3.0 V (unless otherwise noted). The times listed here do not include software overhead.

Parameter	Min	Typ	Max	Unit
MCU, Reset to Active(1)		850 - 3000		us
MCU, Shutdown to Active(1)		850 - 3000		us
MCU, Standby to Active		160		us
MCU, Active to Standby		36		us
MCU, Idle to Active		14		us

(1) The wakeup time is dependent on remaining charge on VDDR capacitor when starting the device, and thus how long the device has been in Reset or Shutdown before starting up again.

5.9 Power consumptions - Power Modes

Table 14: Power consumptions(T_C = 25 °C, V_{DDS} = 3.0 V with DC/DC enabled)

Parameter		Test Conditions	Typ	Unit
WAKEUP AND TIMING				
I_{core}	Reset and Shutdown	Reset. RESET_N pin asserted or VDDS below power-on-reset threshold	150	nA
		Shutdown. No clocks running, no retention	150	
	Standby without cache retention	RTC running, CPU, 80KB RAM and (partial) register retention. RCOSC_LF	0.94	µA
		RTC running, CPU, 80KB RAM and (partial) register retention XOSC_LF	1.09	µA
	Standby with cache retention	RTC running, CPU, 80KB RAM and (partial) register retention. RCOSC_LF	3.2	µA
		RTC running, CPU, 80KB RAM and (partial) register retention. XOSC_LF	3.3	µA
	Idle	Supply Systems and RAM powered RCOSC_HF	675	µA
	Active	MCU running CoreMark at 48 MHz RCOSC_HF	3.39	mA
Peripheral Current Consumption				
I_{peri}	Peripheral power domain	Delta current with domain enabled	97.2	uA
	Serial power domain	Delta current with domain enabled	7.2	
	RF Core	Delta current with power domain enabled, clock enabled, RF core idle	210.9	
	µDMA	Delta current with clock enabled, module is idle	63.9	
	Timers	Delta current with clock enabled, module is idle (1)	81.0	
	I2C	Delta current with clock enabled, module is idle	10.1	
	I2S	Delta current with clock enabled, module is idle	26.3	
	SSI	Delta current with clock enabled, module is idle	82.9	
	UART	Delta current with clock enabled, module is idle (2)	167.5	
	CRYPTO (AES)	Delta current with clock enabled, module is idle (3)	25.6	
	PKA	Delta current with clock enabled, module is idle	84.7	
	TRNG	Delta current with clock enabled, module is idle	35.6	
Sensor Controller Engine Consumption				
I_{sce}	Active mode	24 MHz, infinite loop	808.5	uA
	Low-power mode	2 MHz, infinite loop	30.1	

(1) Only one GPTimer running
(2) Only one UART running
(3) Only one SSI running

5.10 Power consumptions - Radio Modes

Table 15: Power consumptions(T_C = 25 °C, V_{DDS} = 3.0 V with DC/DC enabled)

Parameter		Test Conditions	Typ	Unit
	Radio receive current	2440 MHz	6.9	mA
	Radio transmit current	0 dBm output power setting 2440 MHz	7.3	mA
		+5 dBm output power setting 2440 MHz	9.6	

5.11 Thermal Resistance Characteristics

Table 16: Thermal Resistance Characteristics

Thermal Metric (1)		Package (36 Pins)	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance	23.4	°C/W(2)
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	13.3	°C/W(2)
$R_{\theta JB}$	Junction-to-board thermal resistance	8.0	°C/W(2)
ψ_{JT}	Junction-to-top characterization parameter	0.1	°C/W(2)
ψ_{JB}	Junction-to-board characterization parameter	7.9	°C/W(2)
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.7	°C/W(2)

(1) For more information about traditional and new thermal metrics,
(2) °C/W = degrees Celsius per watt.

6. MSL & ESD

Table 17: MSL and ESD

Parameter	Test Conditions		Value
MSL grade:	MSL 3(1)		
ESD grade:	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (2)	All pins	±2000V
	Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002 (3)	All pins	±500V

(1)The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7. RECOMMENDED TEMPERATURE REFLOW PROFILE

Prior to any reflow, it is important to ensure the modules were packaged to prevent moisture absorption. New packages contain desiccate (to absorb moisture) and a humidity indicator card to display the level maintained during storage and shipment. If directed to bake units on the card, please check the Picture below and follow instructions specified by IPC/JEDEC J-STD-033.

Note: The shipping tray cannot be heated above 65°C. If baking is required at the higher temperatures displayed in the Picture below, the modules must be removed from the shipping tray.

Any modules not manufactured before exceeding their floor life should be re-packaged with fresh desiccate and a new humidity indicator card. Floor life for MSL (Moisture Sensitivity Level) 3 devices is 168 hours in ambient environment 30°C/60%RH.

Table 18: Recommended baking times and temperatures

MSL	125°C Baking Temp.		90°C/≤ 5%RH Baking Temp.		40°C/ ≤ 5%RH Baking Temp.	
	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%
3	9 hours	7 hours	33 hours	23 hours	13 days	9 days

Feasycom surface mount modules are designed to be easily manufactured, including reflow soldering to a PCB. Ultimately it is the responsibility of the customer to choose the appropriate solder paste and to ensure oven temperatures during reflow meet the requirements of the solder paste. Feasycom surface mount modules conform to J-STD-020D1 standards for reflow temperatures.

The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder reflow.

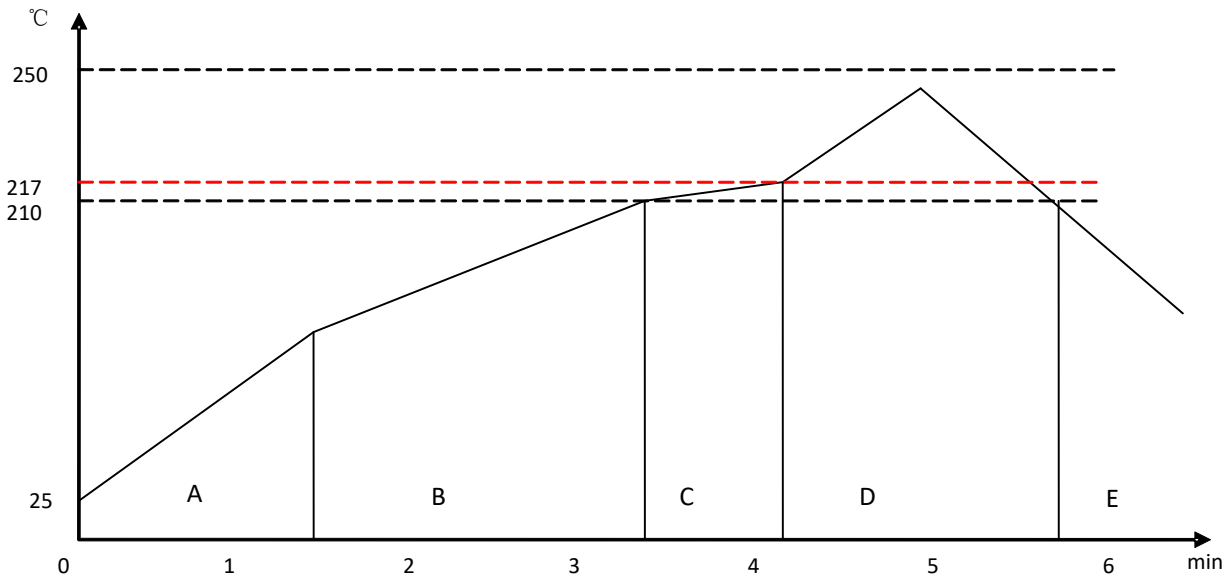


Figure 8: Typical Lead-free Re-flow

Pre-heat zone (A) — This zone raises the temperature at a controlled rate, **typically 0.5 – 2 °C/s**. The purpose of this zone is to preheat the PCB board and components to 120 ~ 150 °C. This stage is required to distribute the heat

uniformly to the PCB board and completely remove solvent to reduce the heat shock to components.

Equilibrium Zone 1 (B) — In this stage the flux becomes soft and uniformly encapsulates solder particles and spread over PCB board, preventing them from being re-oxidized. Also with elevation of temperature and liquefaction of flux, each activator and rosin get activated and start eliminating oxide film formed on the surface of each solder particle and PCB board. **The temperature is recommended to be 150° to 210° for 60 to 120 second for this zone.**

Equilibrium Zone 2 (C) (optional) — In order to resolve the upright component issue, it is recommended to keep the temperature in 210 – 217 ° for about 20 to 30 second.

Reflow Zone (D) — The profile in the figure is designed for Sn/Ag3.0/Cu0.5. It can be a reference for other lead-free solder. The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint. The recommended peak temperature (Tp) is 230 ~ 250 °C. The soldering time should be 30 to 90 second when the temperature is above 217 °C.

Cooling Zone (E) — The cooling ate should be fast, to keep the solder grains small which will give a longer-lasting joint. **Typical cooling rate should be 4 °C.**

8. MECHANICAL DETAILS

8.1 Mechanical Details

- Dimension: 13mm(W) x 26.9mm(L) x 2.0 mm(H) Tolerance: ±0.1mm
- Module size: 13mm X 26.9mm Tolerance: ±0.2mm
- Pad size: 1mmX0.8mm Tolerance: ±0.1mm
- Pad pitch: 1.5mm Tolerance: ±0.1mm

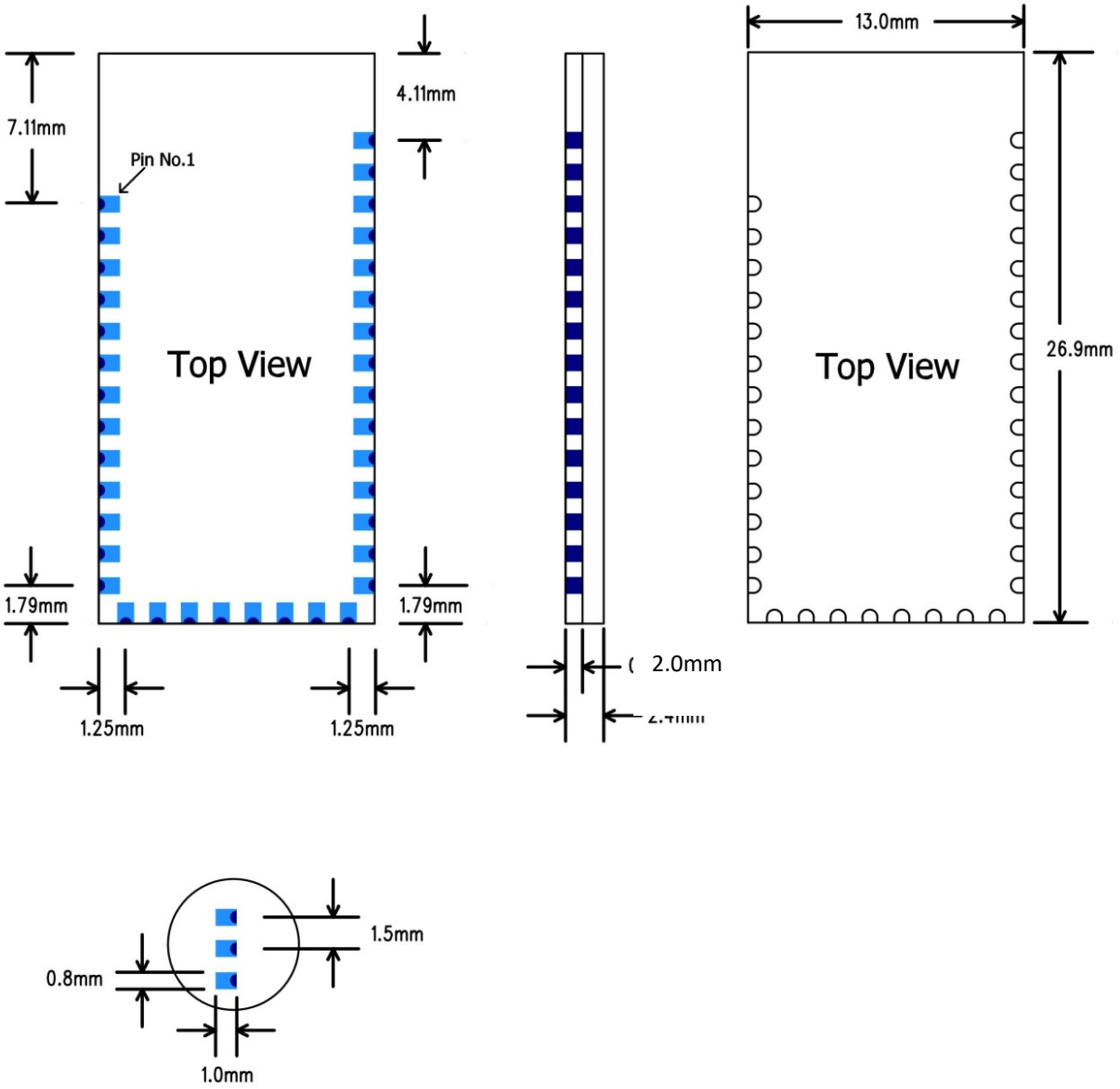


Figure 9: FSC-BT618 footprint

8.2 Host PCB Land Pattern and Antenna Keep-out for FSC-BT618

Please check the picture below for Pad Structure and Keep Out Area:

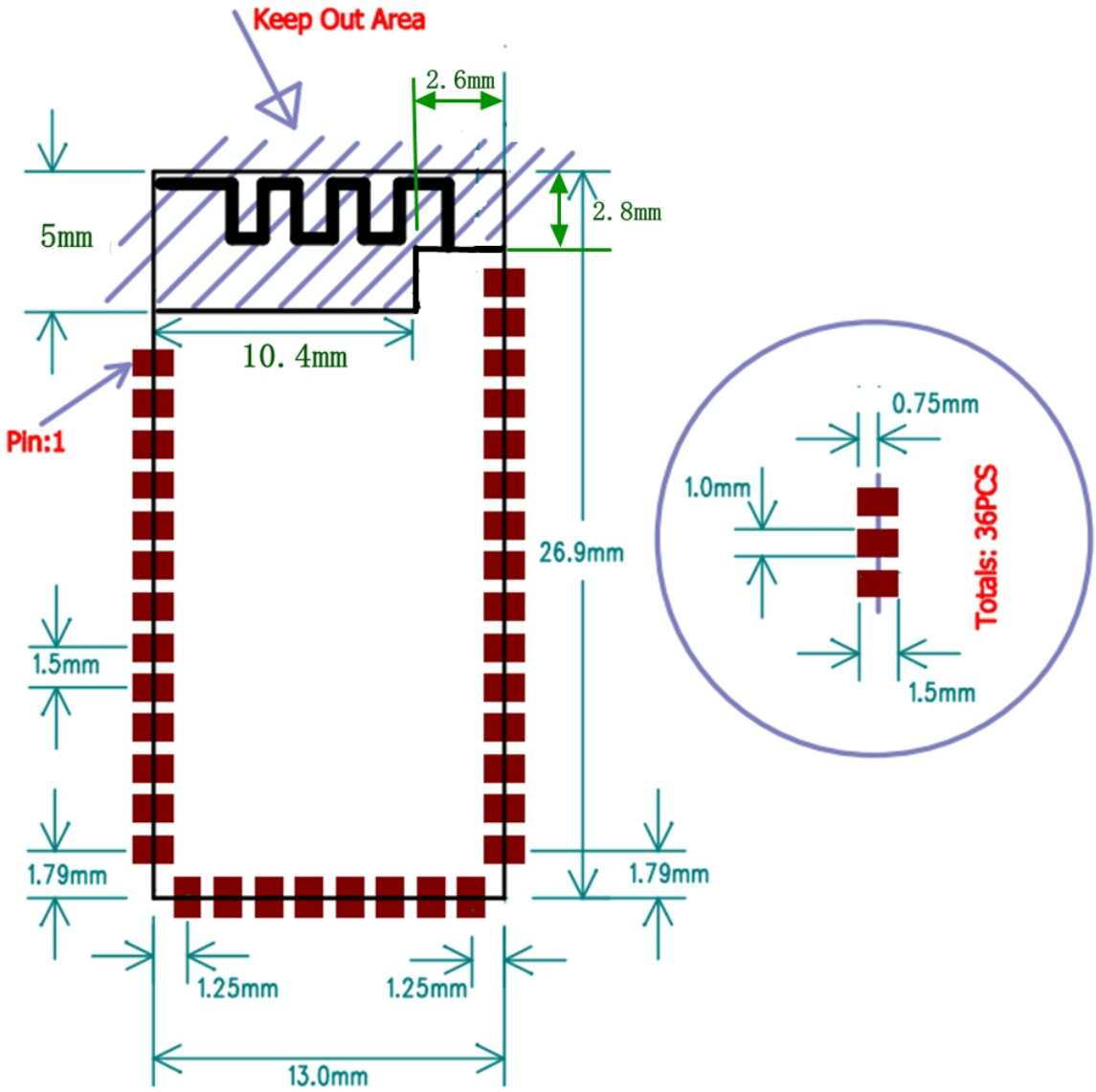


Figure 10: Host PCB-Top View

9. HARDWARE INTEGRATION SUGGESTIONS

9.1 Soldering Recommendations

FSC-BT618 is compatible with industrial standard reflow profile for Pb-free solders. The reflow profile used is dependent on the thermal mass of the entire populated PCB, heat transfer efficiency of the oven and particular type of solder paste used. Consult the datasheet of particular solder paste for profile configurations.

Feasycom will give following recommendations for soldering the module to ensure reliable solder joint and operation of the module after soldering. Since the profile used is process and layout dependent, the optimum profile should be studied case by case. Thus following recommendation should be taken as a starting point guide.

9.2 Layout Guidelines(Internal Antenna)

It is strongly recommended to use good layout practices to ensure proper operation of the module. Placing copper or any metal near antenna deteriorates its operation by having effect on the matching properties. Metal shield around the antenna will prevent the radiation and thus metal case should not be used with the module. Use grounding vias

separated max 3 mm apart at the edge of grounding areas to prevent RF penetrating inside the PCB and causing an unintentional resonator. Use GND vias all around the PCB edges.

The mother board should have no bare conductors or vias in this restricted area, because it is not covered by stop mask print. Also no copper (planes, traces or vias) are allowed in this area, because of mismatching the on-board antenna.

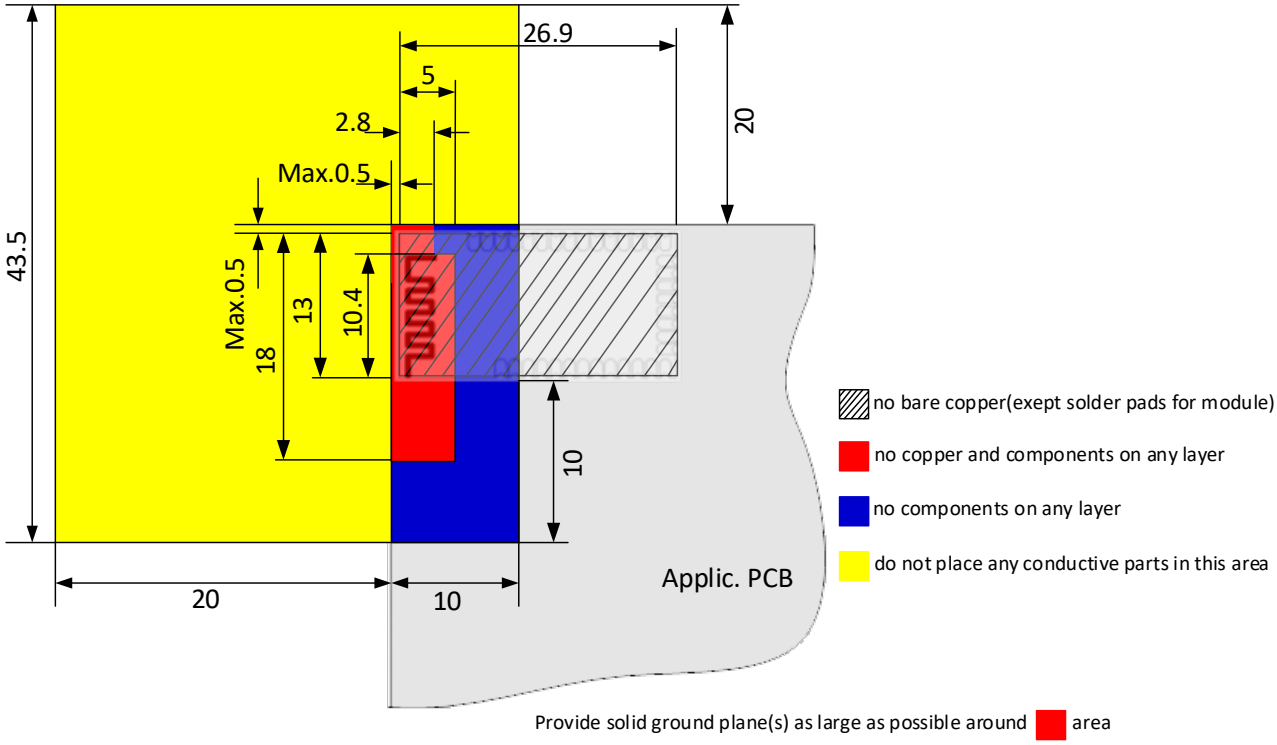


Figure 11: FSC-BT618 Restricted Area (Unit： mm)

Following recommendations helps to avoid EMC problems arising in the design. Note that each design is unique and the following list do not consider all basic design rules such as avoiding capacitive coupling between signal lines. Following list is aimed to avoid EMC problems caused by RF part of the module. Use good consideration to avoid problems arising from digital signals in the design.

Ensure that signal lines have return paths as short as possible. For example if a signal goes to an inner layer through a via, always use ground vias around it. Locate them tightly and symmetrically around the signal vias. Routing of any sensitive signals should be done in the inner layers of the PCB. Sensitive traces should have a ground area above and under the line. If this is not possible, make sure that the return path is short by other means (for example using a ground line next to the signal line).

9.3 Layout Guidelines(External Antenna)

Placement and PCB layout are critical to optimize the performances of a module without on-board antenna designs. The trace from the antenna port of the module to an external antenna should be 50Ω and must be as short as possible to avoid any interference into the transceiver of the module. The location of the external antenna and RF-IN port of the module should be kept away from any noise sources and digital traces. A matching network might be needed in between the external antenna and RF-IN port to better match the impedance to minimize the return loss.

As indicated in picture below, RF critical circuits of the module should be clearly separated from any digital circuits on the system board. All RF circuits in the module are close to the antenna port. The module, then, should be placed in this way that module digital part towards your digital section of the system PCB.

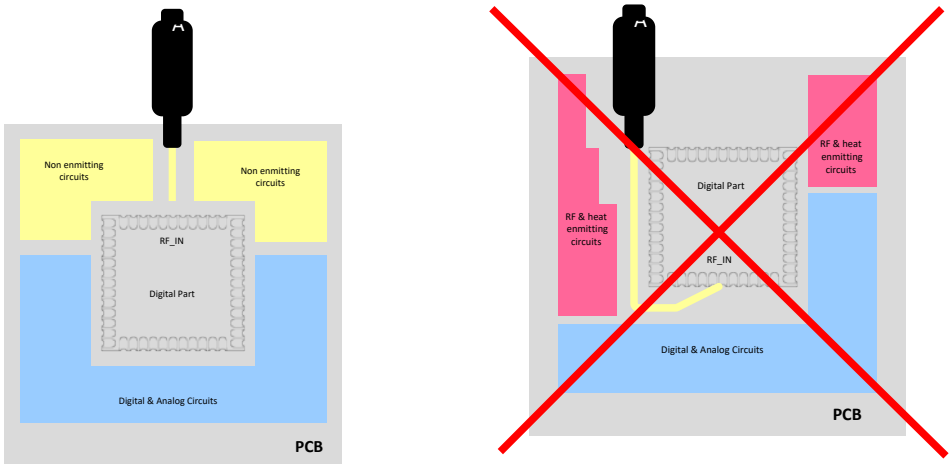


Figure 12: Placement the Module on a System Board

9.3.1 Antenna Connection and Grounding Plane Design

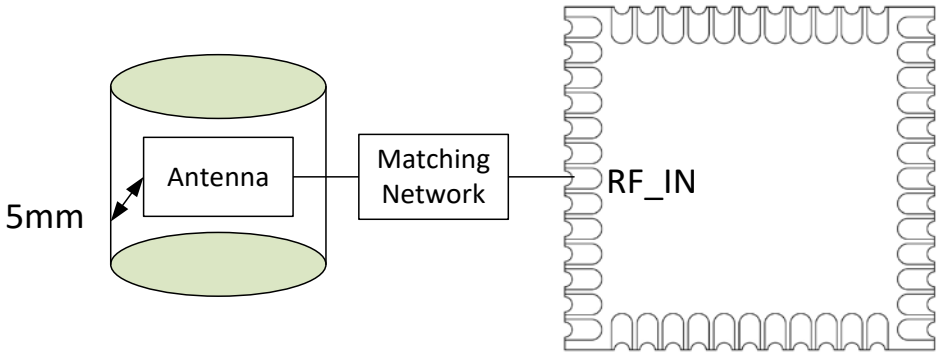


Figure 13: Leave 5mm Clearance Space from the Antenna

General design recommendations are:

- The length of the trace or connection line should be kept as short as possible.
- Distance between connection and ground area on the top layer should at least be as large as the dielectric thickness.
- Routing the RF close to digital sections of the system board should be avoided.
- To reduce signal reflections, sharp angles in the routing of the micro strip line should be avoided. Chamfers or fillets are preferred for rectangular routing; 45-degree routing is preferred over Manhattan style 90-degree routing.

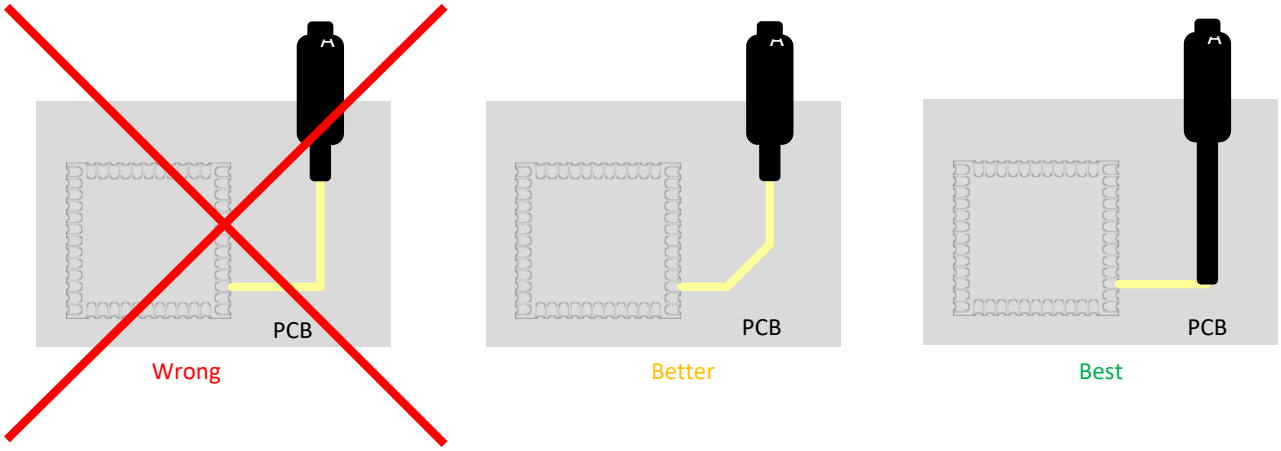


Figure 14: Recommended Trace Connects Antenna and the Module

- Routing of the RF-connection underneath the module should be avoided. The distance of the micro strip line to the ground plane on the bottom side of the receiver is very small and has huge tolerances. Therefore, the impedance of this part of the trace cannot be controlled.
- Use as many vias as possible to connect the ground planes.

10. PRODUCT PACKAGING INFORMATION

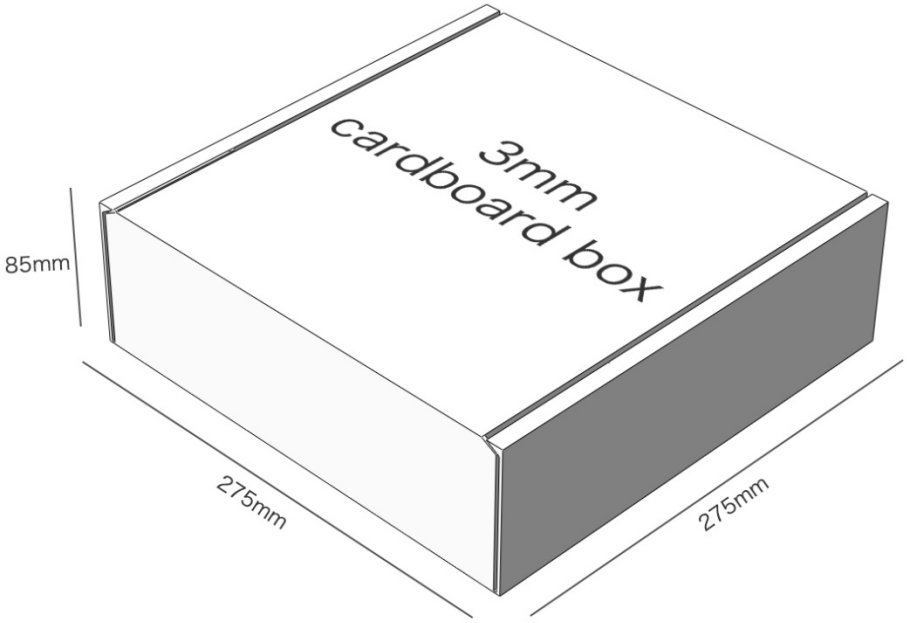
10.1 Default Packing

a, Tray vacuum

b, Tray Dimension: 180mm * 195mm

Figure 15: Tray vacuum

10.2 Packing box(Optional)



* If require any other packing, must be confirmed with customer

* Package: 1000PCS Per Carton (Min Carton Package)

Figure 16: Packing Box

12. APPLICATION SCHEMATIC